caused by the warp of the base member, thereby reducing the mounting failure rate. Therefore, the object of the present invention is different from Tetsuo.

According to the present invention, an entire area of the base member is covered by the interconnect layer and the floating electrically conductive layer. As a result, penetration of moisture can be prevented.

In contrast, Tetsuo is silent on the penetration of moisture which can cause problems if there is a surface exposed to such moisture. Furthermore, in Tetsuo, the generation of a crack cannot be prevented when a chip is mounted during the mounting operation.

Claims 2-3 were rejected under 35 U.S.C. §103(a) as being unpatentable over Tetsuo, and further in view of Asai et al., U.S. Patent No. 6,411,519, hereinafter referred to as Asai. Asai has an effective reference date of the filing date of its parent application on May 31, 2000, (column 1, lines 3-4), and **not** the filing date of the International Application from which it was derived on September 28, 1998, (column 1, lines 4-6; see 35 U.S.C. §102(e)(2)). Therefore, a certified English translation of the priority document herein, Japanese Patent Application No. 2000-016168, filed on January 25, 2000, is enclosed herewith, and this causes the effective date of this application to antedate the effective date of Asai on May 31, 2000.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

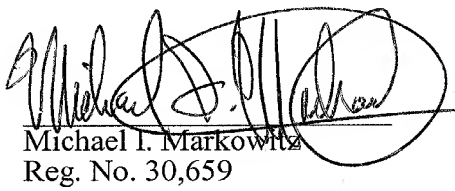
CLOSING

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claim 1 is in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



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Reg. No. 30,659

Enclosure: Version With Markings to Show Changes Made
Certified English Translation of Japanese Patent Application No. 2000-016168

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph beginning on page 11, line 22, and ending on page 12, line 6, has been rewritten as follows:

As shown Fig. 8 [illustrating] illustrates a circuit board of a fourth embodiment, the circuit board 81 has a triple layered interconnect structure, that is, includes a top interconnect layer (not shown) on the top surface of the base member 12 having the same configuration as that of the first embodiment, and a first bottom interconnect layer 82 and a second bottom interconnect layer 83 on the bottom surface of the base member 12. The circuit board 81 further includes a floating conductive layer 84, a first dielectric layer 85 and a second dielectric layer [86.] 88.

The paragraph on page 12, lines 9-13, has been rewritten as follows:

The second bottom interconnect layer 83 is disposed overlying the first bottom interconnect layer 82 and the first dielectric layer 85 and sandwiching the second dielectric layer [86,] 88, or disposed between the base member 12 and the second dielectric layer [86.] 88.

The paragraph beginning on page 12, line 25, and ending on page 13, line 3, has been rewritten as follows:

The first dielectric layer 85 partially covers the first bottom interconnect layer 82 and sandwiches, with the floating conductive layer 84 and the second bottom interconnect layer 83, the second dielectric layer [86.] 88.

The paragraph on page 13, lines 10-17, has been rewritten as follows:

In the present embodiment, the generation of the crack "C" in the second dielectric layer [86] 88 between the base member 12 and the first dielectric layer 85 is suppressed by the presence of the floating conductive layer 84, or the floating conductive layer 84 acts as a crack stopper for the second dielectric layer [86.] 88. Accordingly, the thickness of the entire circuit board can be reduced similarly to the first embodiment.

IN THE CLAIMS

Claims 2 and 3 have been rewritten as follows:

2. (Once Amended) The circuit board as defined in claim 1, wherein [a pair of the interconnect layers are disposed on each of both surfaces of the base member.] the interconnect layer comprises a top interconnect layer on a top surface of the base member and a bottom interconnect layer on a bottom surface of the base member.

3. (Once Amended) The circuit board as defined in claim 2, wherein [volumes of the pair of the interconnect layers] a volume of the top interconnect layer and a volume of the bottom interconnect layer are substantially [same.] equal.